Product Brief

GRF6504
PHS RF CMOS Transceiver

GRF6504 Features

- True single-chip CMOS RF transceiver
  - Integrated LNA fully covering international 1.9 GHz PHS band
  - Fully integrated transmitter with programmable output power
  - Built-in channel selection filter
  - Fully integrated sigma-delta fractional-N frequency synthesizer including VCO and loop filters
  - Integrated I/Q up/down conversion mixer (1.2MHz of IF signals)
  - Programmable gain stage in Rx
  - Programmable output power in Tx

- Low-cost CMOS process technology with high performance
  - Allow under -104dBm min-sen (typ)
  - NF ~ 5.5dB, IIP3 ~ -15.5 dBm (typ.)

- Small form factor
  - 48pin 7mm x 7mm QFN

- Low power consumption
  - Tx: 50 mA at 2.8V, Rx: 100mA at 3.0V (typ)

- Fast switching time
  - Support seamless handover
  - Less than 25 us switching time: channel switching, Tx, Rx switching

- High performance ultra fast-lock PLL
  - Phase noise: -118dBc/Hz at 600kHz offset (typ)
  - Fast channel switching time: 20 us (typ)

- Analog base-band interface
  - Tx: Zero-IF I/Q differential
  - Rx: 1.2 MHz IF output
  - 3-wire program interface
  - RSSI output

- Supply voltage from 2.7V to 3.3V

GRF6504 Benefits

- Most cost-effective PHS RF transceiver
  - TRUE single-chip transceiver
  - Lowest BOM count < 50 components

- Extends frequency bands to support many nations including Japan, China, India, Mexico and Vietnam

- Outstanding performance per cost
  - Good sensitivity performance for mobile applications
  - Considerable RF performance margins for mobile applications
  - Longer battery-life

- Easy design and interface

Description

GCT’s GRF6504 is a highly integrated monolithic RF transceiver for PHS applications based on GCT’s industry proven CMOS RF technologies. This transceiver includes GCT’s intrinsic low-IF (intermediate frequency) radio technology and requires a minimum number of external components, resulting in lower BOM cost and a smaller PCB area.

GRF6504 is housed in 48-pin 7mmx7mm QFN package.

GRF6504 consists of a receiver, a transmitter, and PLL. The receiver section includes all functional blocks from the RF front-end to the base-band interface; LNA for 1.9GHz bands, down-conversion mixers, base-band filters, gain-controlled amplifiers and analog 1.2MHz IF interface. The transmitter section uses I/Q up-conversion architecture including analog base-band I/Q interface, up-conversion mixers and preamplifiers. The on-chip PLL includes VCO, a sigma-delta fractional-N frequency synthesizer, and built-in loop filters meeting fast and stable switching time requirements.
Applications
- PHS mobile devices

Simplified Application Block Diagram